

REMARKS

Claims 1-3 are all the claims pending in the application.

Claims 1 and 3 are rejected under 35 U.S.C. § 102(e) as anticipated by Gupta (U.S. Patent No. 5,996,083); and claim 2 is rejected under 35 U.S.C. § 103(a) as obvious over Gupta. Reconsideration and removal of these rejections are respectfully requested on the basis of the present amendment to the claims and the following remarks.

Applicants' invention is a programmable controller for controlling a controlled apparatus by pulse output, where the controller has a pulse generating section for outputting a pulse string having a set cycle, and a pulse dividing section for dividing the pulse string output from the pulse generating section at a predetermined dividing ratio. The pulse dividing section outputs an interruption request signal having a cycle which is n times (n is a positive integer) as great as the cycle of the pulse string. A central processing unit executes interrupt processing in response to the interruption request signal output from the pulse dividing section so as to control the output of the pulse generating section.

Gupta is intended to provide a microprocessor having software controllable power consumption which adjusts the rate of execution of a functional unit by removing power to the functional unit so that the power consumption is reduced. As shown in Fig. 3, a global power control register field 140 adjusts the rate of execution of all the functional units by controlling the clock frequency supplied to all the functional units. A clock divider 128 divides down the master clock signal responsive to the value stored in the power control register field 140.

While the clock divider 128 disclosed by Gupta produces a system clock signal that is distributed over the CPU 100 via the clock tree 132, Gupta does not disclose that the pulse dividing section outputs an interruption request signal to the CPU which, in turn, controls the output of the pulse generating section by executing interrupt processing in response to the interruption request signal output from the pulse dividing section as called for in the present claim 1. In Gupta, the power control register 106 (CPU) does not control the output of the clock generator 130 in response to the system clock signal. Thus, claim 1 is not anticipated by, or obvious over, Gupta.

Amended claim 1 patentably distinguishes over the Gupta reference for the reason discussed above. Dependent claims 2 and 3, due to dependency, also patentably distinguishes over Gupta for at least the reason that their base claim 1 patentably distinguishes over the cited art.

Attached hereto is a version with markings to show changes made.


In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

AMENDMENT UNDER 37 C.F.R. § 1.111
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Respectfully submitted,


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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 8, paragraph 1:

In the second embodiment, the constant interruption cycle for the CPU 1 is maintained irrespective of a change in an output frequency. Therefore, even if the output pulse cycle is increased, the ~~responsivity~~response of the processing other than the pulse output is not deteriorated.

IN THE CLAIMS:

The claims are amended as follows:

1. (Amended) A programmable controller for controlling a controlled apparatus by pulse output, comprising:

a pulse generating section for outputting a pulse string having a set cycle;

a pulse dividing section for dividing the pulse string output from said pulse generating section ~~and~~ at a predetermined dividing ratio and for outputting an interruption request signal having a cycle which is n times (~~n is a positive integer~~) as great as the cycle of the pulse string;

where n is a positive integer; and

AMENDMENT UNDER 37 C.F.R. § 1.111
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a central processing unit for executing an interruption processing in response to the interruption request signal output from said pulse dividing section s as to control the output of said pulse generating section.